

DFM analysis report_JLCDFM

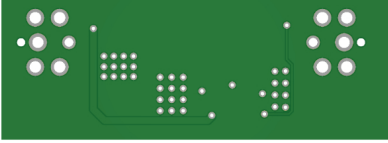
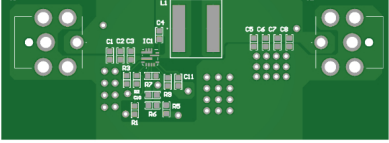
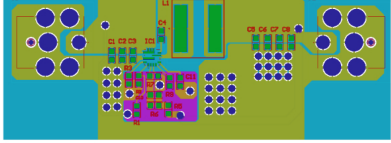
File name: Project Outputs for Barrel Jack DCDC Project.zip

Report generated at: 2024-09-09 16:56:47

PCB layers: 4Layer

PCB size: 7.48x2.82cm

Analyze project: ☒ PCB DFM ☐ SMT DFM



PCB DFM>Routing layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Sharp trace corner (Check for sharp corners in traces)	No	No	No	Danger: 0 Warning: 0 Good: 0
BGA pad (Check BGA pads on the board)	No	No	No	Danger: 0 Warning: 0 Good: 0
Via placed within a pad (Check if there is a via placed within a pad)	No	No	No	Danger: 0 Warning: 0 Good: 0
Trace to board edge (Detect traces too close to the board edge)	No	No	No	Danger: 0 Warning: 0 Good: 0
Trace spacing (Measure spacing between adjacent parallel traces)	No	No	No	Danger: 0 Warning: 0 Good: 0
Unconnected trace end (Free-standing trace ends not connected to pads)	No	No	No	Danger: 0 Warning: 0 Good: 0
Trace width (Trace width information)	0.25mm Good		Project Outputs for Barrel Jack DCDC ProjectPCB2_Copper_Signal_Bot.gbr Project Outputs for Barrel Jack DCDC ProjectPCB2_Copper_Signal_Top.gbr	Danger: 0 Warning: 0 Good: 15
Fiducial (Detect fiducial marks on the board)	No	No	No	Danger: 0 Warning: 0 Good: 0
Pad to board edge (Measure distance of pads from the board edge)	No	No	No	Danger: 0 Warning: 0 Good: 0
Pad spacing (Measure pad to pad spacing)	0.23mm Good		Project Outputs for Barrel Jack DCDC ProjectPCB2_Copper_Signal_Top.gbr	Danger: 0 Warning: 0 Good: 8
Plated through-hole to trace clearance (Measure clearance of plated through-holes to traces)	No	No	No	Danger: 0 Warning: 0 Good: 0
Annular ring (Annular ring width of pads compared to holes)	No	No	No	Danger: 0 Warning: 0 Good: 0
tht to smd (Detect clearance of vias to pads)	0.64mm Danger		Project Outputs for Barrel Jack DCDC ProjectPCB2_Copper_Signal_Top.gbr	Danger: 33 Warning: 17 Good: 0
Via to pad (Detect clearance of vias to pads)	No	No	No	Danger: 0 Warning: 0 Good: 0

PCB DFM>Soldermask layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Soldermask bridge (Detect distance between parallel soldermask opening edges)	0.15mm Good		Project Outputs for Barrel Jack DCDC ProjectPCB2_Soldermask_Top.gbr	Danger: 0 Warning: 0 Good: 5
Solder mask opening exposing trace (Detect clearance of solder mask openings to nearby traces)	No	No	No	Danger: 0 Warning: 0 Good: 0
Soldermask opening with multiple segments (Check if solder mask openings are constructed from multiple geometric shapes)	null Warning		Project Outputs for Barrel Jack DCDC ProjectPCB2_Soldermask_Top.gbr	Danger: 0 Warning: 1 Good: 0
Negative soldermask expansion (Detect solder mask openings smaller than their corresponding pads)	No	No	No	Danger: 0 Warning: 0 Good: 0

PCB DFM>Silkscreen layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Silkscreen to pad (Detect clearance of silkscreen to pads)	No	No	No	Danger: 0 Warning: 0 Good: 0
Silkscreen to hole (Detect clearance of silkscreen to holes)	No	No	No	Danger: 0 Warning: 0 Good: 0
Silkscreen line width (Check silkscreen line width)	0.1mm Danger		Project Outputs for Barrel Jack DCDC ProjectPCB2_Legend_Top.gbr	Danger: 10 Warning: 40 Good: 0

PCB DFM>Drill layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Missing plated through-hole (Detect top and bottom pads at the same location without plated through-holes)	No	No	No	Danger: 0 Warning: 0 Good: 0
Plated through-hole spacing (Measure spacing between plated through-holes)	No	No	No	Danger: 0 Warning: 0 Good: 0
Short slot detection (Detect slots shorter than twice their width)	No	No	No	Danger: 0 Warning: 0 Good: 0
Slot width check (Measure slot width)	No	No	No	Danger: 0 Warning: 0 Good: 0
Via to PTH spacing (Measure spacing of vias to plated through-holes)	No	No	No	Danger: 0 Warning: 0 Good: 0
Unconnected via (Detect isolated unconnected vias)	No	No	No	Danger: 0 Warning: 0 Good: 0